Lecture 9

Main Memory II

Lecture Information

Ceng328 *Operating Systems* at April 20, 2010

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  - Each binding is a mapping from one address space to another.

Address Binding II

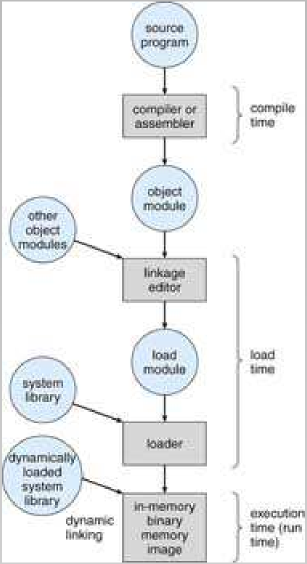

Figure: Multistep processing of a user program.

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- The run-time mapping from virtual to physical addresses is done by a hardware device called the **memory-management unit** (MMU).

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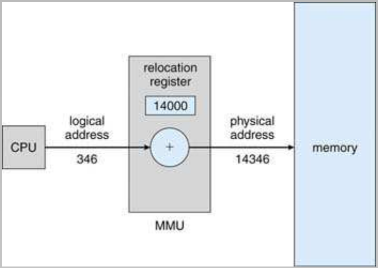

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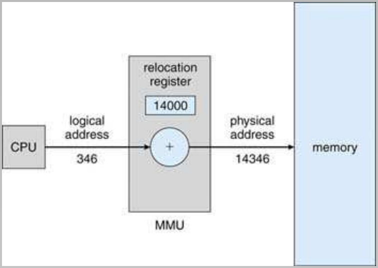

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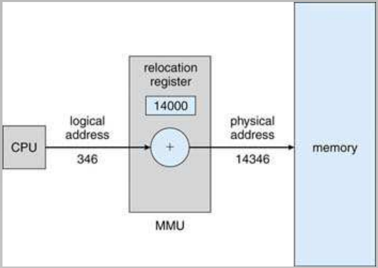

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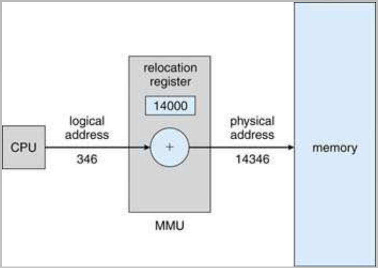

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- The concept of a logical address space that is bound to a separate physical address space is central to proper memory management.

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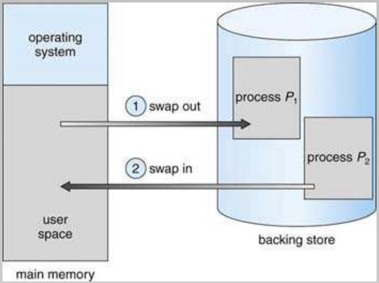

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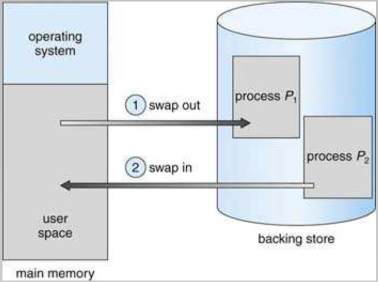

Figure: Swapping of two processes using a disk as a backing store.

- The quantum must be large enough to allow reasonable amounts of computing to be done between swaps.

Swapping II

- Normally, a process that is swapped out will be swapped back into the same memory space it occupied previously.

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    - Swapping is again halted when the load on the system is reduced.

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- In the contiguous memory allocation, each process is contained in a single contiguous section of memory.
- With **relocation** and **limit** registers, each logical address must be less than the limit register;
- The MMU maps the logical address dynamically by adding the value in the relocation register. This mapped address is sent to memory (see Fig. 4).

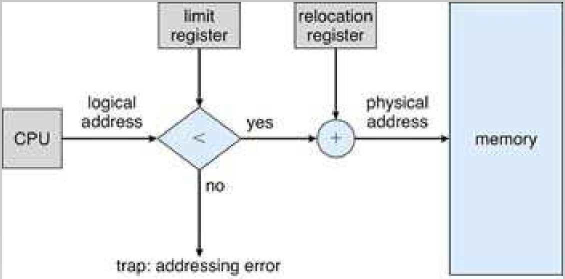

Figure: Hardware support for relocation and limit registers.

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  - Thus, using this code changes the size of the OS during program execution.

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- This method is no longer in use.

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- At any given time, we have a list of available block sizes and the input queue.
- The OS can order the input queue according to a scheduling algorithm.

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- Simulations have shown that both first fit and best fit are better than worst fit in terms of decreasing time and storage utilization.
- Neither first fit nor best fit is clearly better than the other in terms of storage utilization, but first fit is generally faster.

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- The general approach to avoiding this problem is to break the physical memory into fixed-sized blocks and allocate memory in units based on block size.

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- Another possible solution to the external-fragmentation problem is to permit the logical address space of the processes to be **non-contiguous**, thus allowing a process to be allocated physical memory wherever the latter is available.
- Two complementary techniques achieve this solution:
  - paging
  - segmentation
- These techniques can also be combined.

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- However, recent designs have implemented paging by closely integrating the hardware and OS, especially on 64-bit microprocessors.

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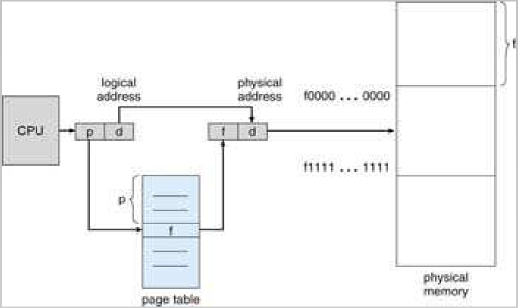

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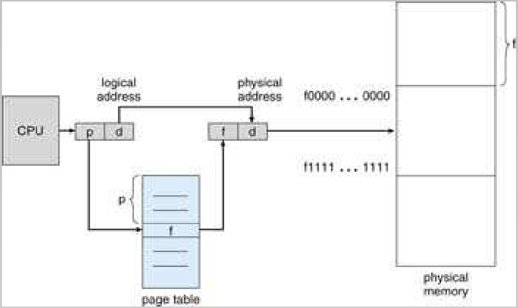

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- The hardware support for paging is illustrated in Fig. 5.

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- The paging model of memory is shown in Fig. 6.

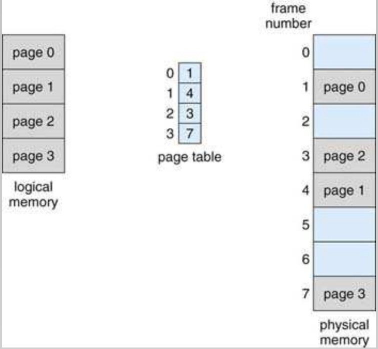

Figure: Paging model of logical and physical memory.

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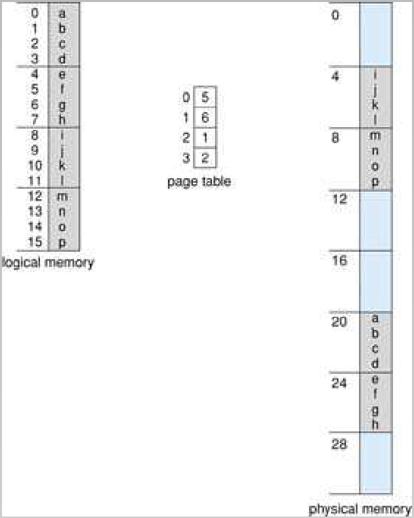

Figure: Paging example for a 32-byte memory with 4-byte pages.

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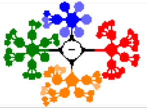

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- If frame size is 4 KB, then a system with 4-byte entries can address $2^{44}(4KB * 2^{32})$ bytes (or 16 TB) of physical memory.

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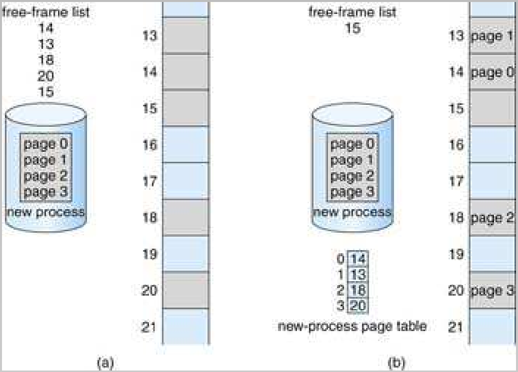

Figure: Free frames (a) before allocation and (b) after allocation.

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- Illegal addresses are trapped by use of the valid-invalid bit.

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- This problem is a result of the 2-KB page size and reflects the internal fragmentation of paging.

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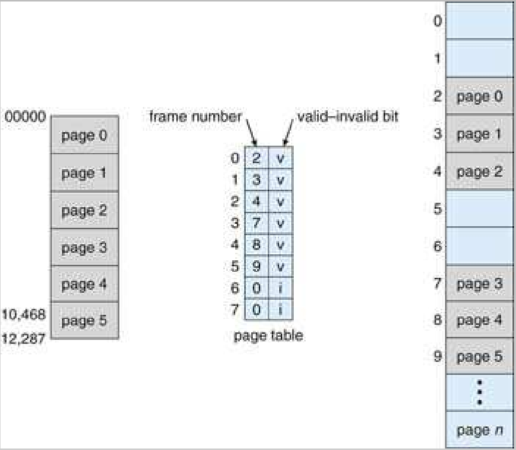

Figure: Valid (v) or invalid (i) bit in a page table.

Shared Pages I

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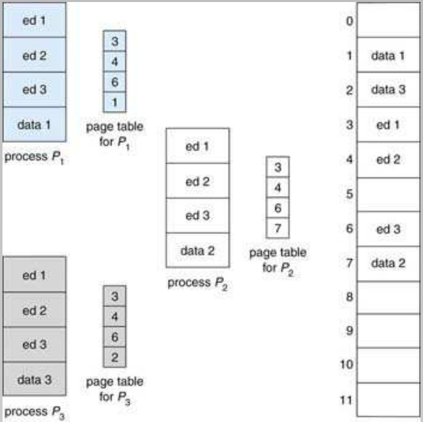

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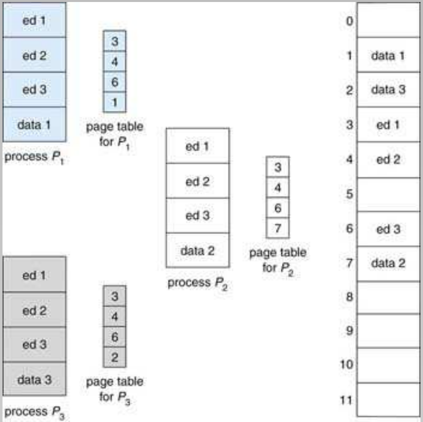

Figure: Sharing of code in a paging environment.

- Consider a system that supports 40 users, each of whom executes a text editor (see Fig. 10).

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- Reentrant code is non-self-modifying code; it never changes during execution.
- Thus, two or more processes can execute the same code at the same time.

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- If the text editor consists of 150 KB of code and 50 KB of data space, we need 8,000 KB to support the 40 users $(40 * (150KB + 50KB))$.
- If the code is reentrant code (or pure code), it can be shared (to be shareable, the code must be reentrant).
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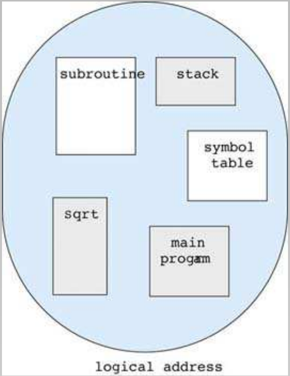
- Thus, to support 40 users, we need only one copy of the editor (150 KB), plus 40 copies of the 50 KB of data space per user.
- The total space required is now 2,150 KB instead of 8,000 KB-a significant savings.

Basic Method I

- Users prefer to view memory as a collection of variable-sized segments, with no necessary ordering among segments (Figure 8.18).



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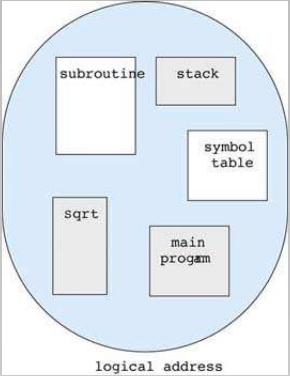

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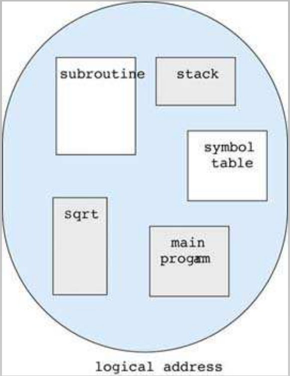

Figure: User's view of a program.

- Segmentation is a memory-management scheme that supports this user view of memory.
- A logical address space is a collection of segments.

Basic Method II

- Each segment has a name and a length. The addresses specify both the segment name and the offset within the segment.

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- This mapping is effected by a **segment table**. Each entry in the segment table has a segment base and a segment limit.
- The segment base contains the starting physical address where the segment resides in memory, whereas the segment limit specifies the length of the segment (see Fig. 12).

Hardware II

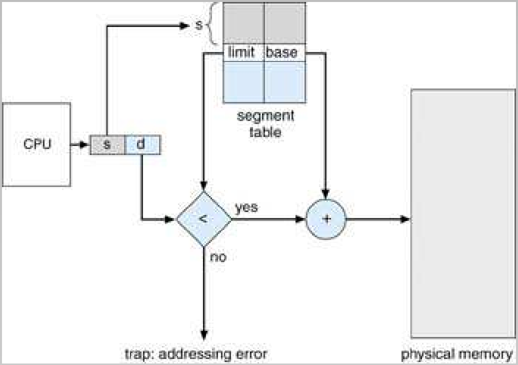

Figure: Segmentation hardware.

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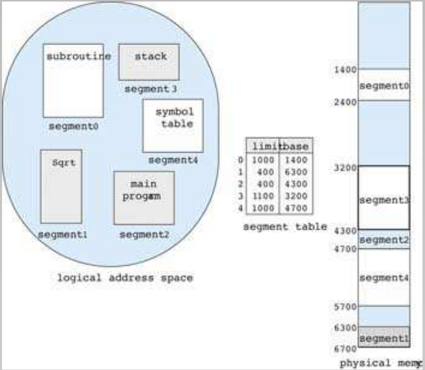
- As an example, consider the situation shown in Fig. 13.

Hardware IV



	limit	base
0	1000	1400
1	400	6300
2	400	4300
3	1100	3200
4	1000	4700

Figure: Example of segmentation.

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- Thus, a reference to byte 53 of segment 2 is mapped onto location 4300 + 53 = 4353.
- A reference to segment 3, byte 852, is mapped to 3200 (the base of segment 3) + 852 = 4052.
- A reference to byte 1222 of segment would result in a trap to the OS, as this segment is only 1,000 bytes long.